Amendments to the Specification:

Please replace the paragraph beginning on page 6, line 12 with the following amended paragraph:

FIG. 1 is a schematic block diagram of an embedded DRAM memory and test system according to a first embodiment of the present invention. In FIG. 1, embedded DRAM **100** comprises a multiplicity of DRAM blocks **105A, 105B, 105C** through **105N**. DRAM block **105A** being the first DRAM block and DRAM block **105N** being the last block of embedded DRAM **100** in terms of address sequence. While FIG. 1 illustrates DRAM blocks **105A** through **105N** arranged in a stack of one above another, the physical layout of the DRAM blocks may be different, for example, the DRAM blocks may be arranged into two adjacent stacks. Embedded DRAM **100** is coupled to a built in self-test (BIST) system **110**. A BIST based tester for an embedded DRAM is described in United States Patent 5, 961,653 which is hereby incorporated by reference. BIST system 110 and embedded DRAM 100 are preferably embodied in an integrated circuit chip. Test system **110** is comprised of a sequencer **115**, an address generator **120**, a test data generator **125**, a controller **130**, a multiplexer **135**, a comparator **140**, redundancy allocation logic **145** and a redundancy allocation register **150** all coupled to a test bus **155**. Alternatively, sequencer **135** may be incorporated in DRAM **100**.